# A Network Processor based Internet Protocol Router for a Third Generation Mobile System

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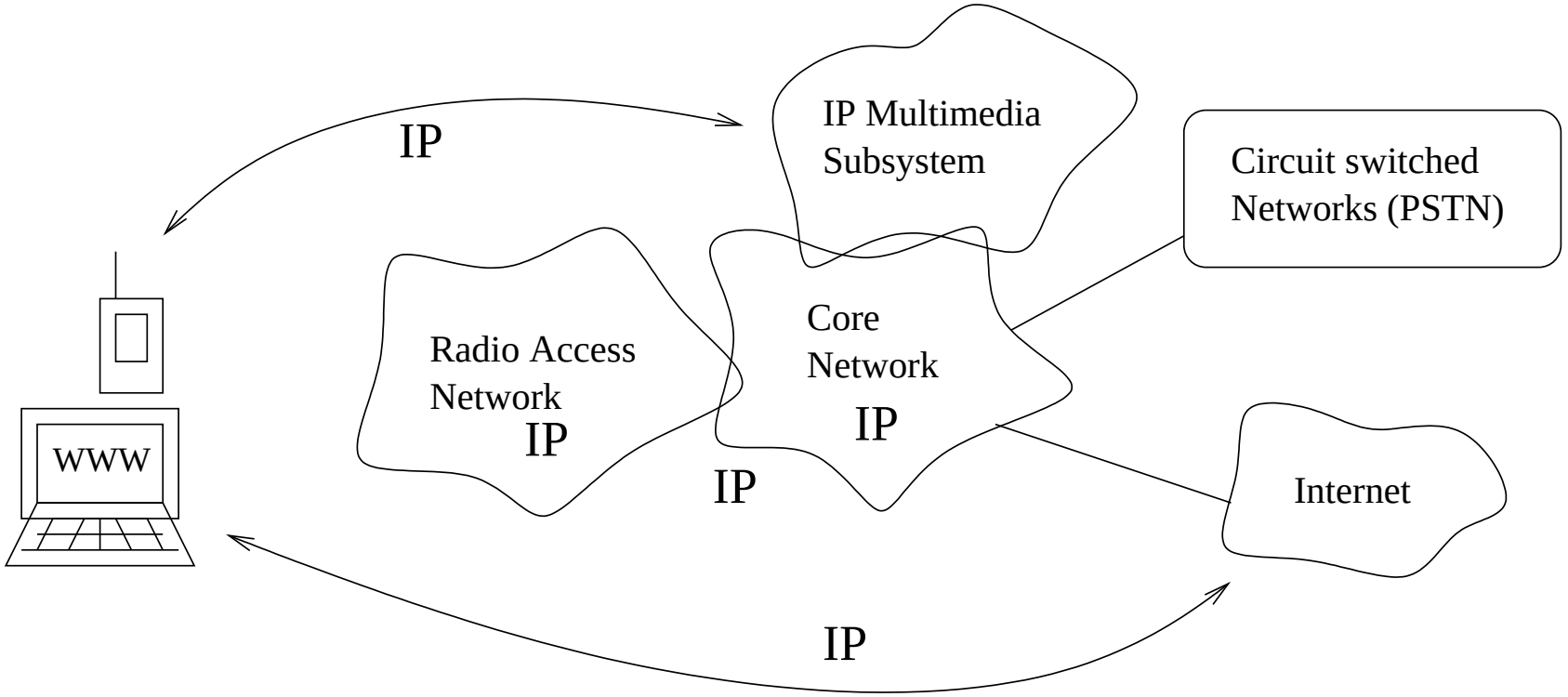
# Background (1/2)

- IP in user terminals
- IP in transport networks as a data and signal bearer



# Background (2/2)

- Data rates and volumes are growing
- Various quality, capacity and speed requirements
- More intelligent and faster routers are required
- SW based solution: Flexible, Poor performance
- ASIC based solution: Expensive, Inflexible
- Network processor: Programmable, Optimised for packet processing

# Problem Description

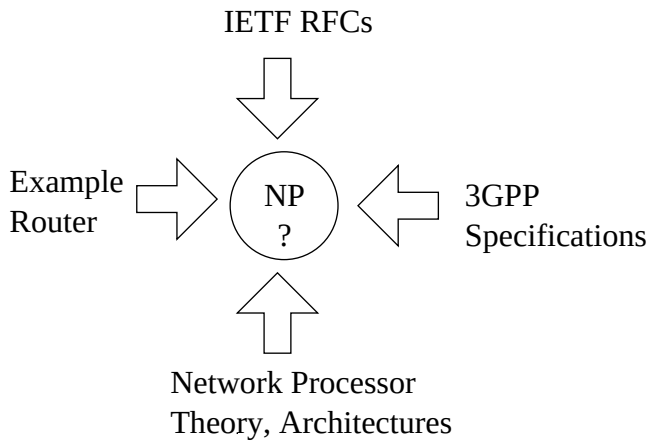
Study the usage and the feasibility of using a network processor based IP routing device in a Third Generation Partnership Project (3GPP) compliant network.

## Scope

- 3GPP transport network layer in UTRAN and CS- and PS-core network
- IP routing. (No higher level processing)

# Methods

- Studying standards and requirements:
  - Internet Protocol: RFCs from IETF
  - 3GPP specifications and reports
- Studying network processor theory and architectures
- Implementing an example IP router using a network processor simulator



## Own contribution

- Literature study: IETF, 3GPP, Network processor literature and white papers. (Biggest part)
- Example router implementation: Specification, Design, Implementation, Simulation. (Based heavily on existing code from the reference material)

# Internet Protocol (1/4)

| | |
|---|---|
| Application layer | Telnet, FTP, SMTP, ... |
| Transport layer | TCP, UDP, SCTP |
| Internet layer | IP, ICMP, IGMP, IPv6 |
| Link layer | address resolution, IP encapsulation |

Study focus was on internet and link layers.

# Internet Protocol (2/4)

Following topics were studied:

- IPv4, ICMP, IPv6, (*no* multicast)
- IP over ATM, Ethernet, ARP
- UDP, TCP
- Quality of Service: Diffserv, Intserv
- briefly mentioned SCTP, IPSec, PPP

# Internet Protocol (3/4)

An important input was the forwarding algorithm from RFC1812:

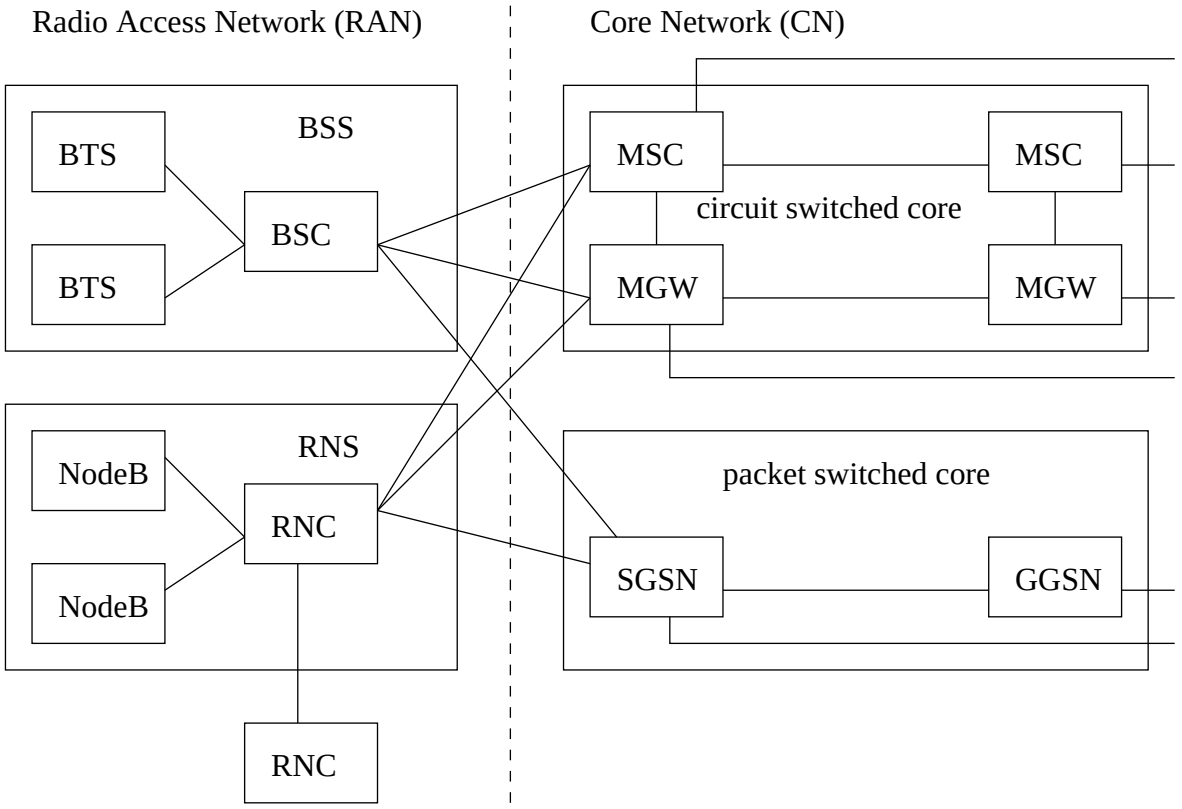
1. Receive a packet from the link layer.
2. Validate the IP header.
3. Process IP options.
4. Decide the next hop IP addresss based on the destination address.
5. Force forwarding constraints.
6. Decrease TTL.
7. Fragment packet if necessary.
8. Determine link layer address based on next hop IP.
9. Encapsulate and send to link layer.

# Internet Protocol (4/4)

Packet processing functions that are required from a router are:

- Address lookup
- Forwarding
- Error detection
- Fragmentation and reassembly
- Protocol demultiplexing, classification
- Queueing and scheduling
- Traffic measurement, policing and shaping

# 3GPP (1/3)




Reviewed IP bearers in RNC, MSC, MGW and GSN.

# 3GPP (2/3)

- IP data and signal bearers:
  - Packet switched data: IP/UDP/GTP
  - Circuit switched data: IP/UDP/RTP
  - Signalling: IP/SCTP/M3UA
  - NodeB data transport: IP/UDP
- Studied RTP, GTP and SS7 protocols
- QoS: configurable Diffserv codepoint marking required
- Interworking: ATM – IP, IPv4 – IPv6, signalling gateways

# 3GPP (3/3)

3GPP standards do not introduce any new requirements. Some IETF requirements are lessened and some others mandated.

Desirable features are support for various link layer techniques: (ATM, Ethernet, PPP) and Diffserv.

# Network processors

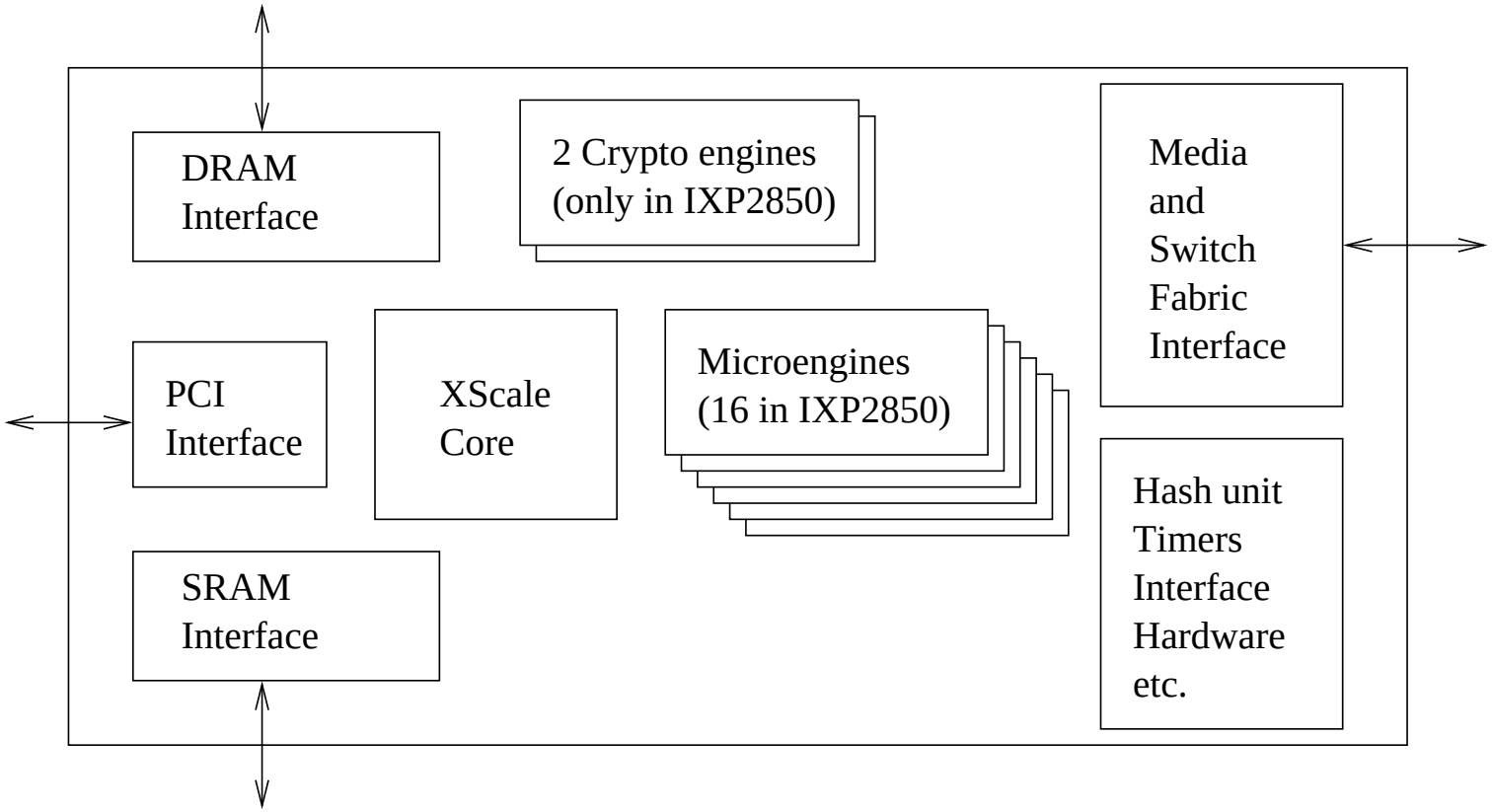
Network processors are a relatively new technology and there are various architectures and companies that offer different solutions.

Network Processor Forum (NPF) develops standards and benchmarks.

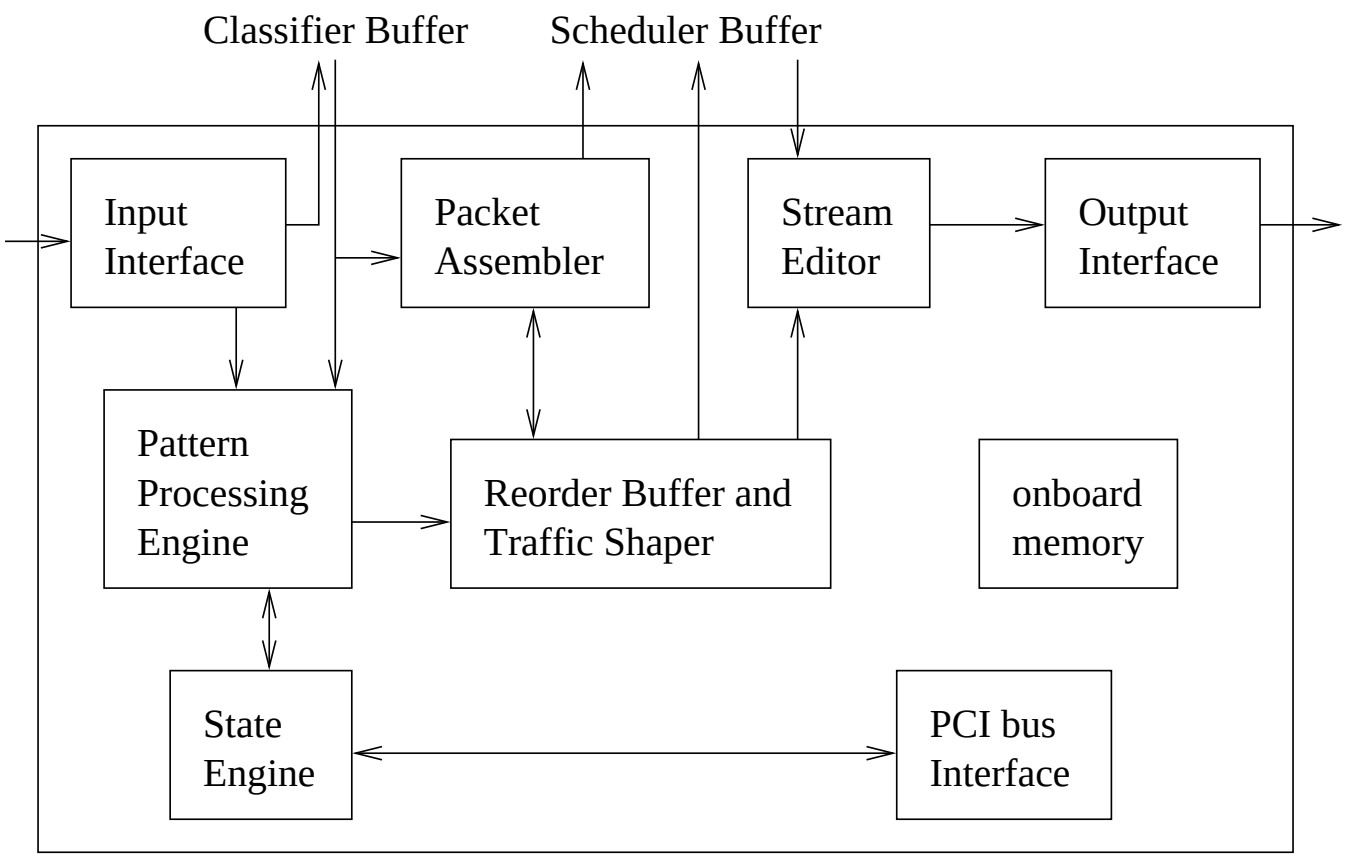
Evaluation should consider *functionality*, *performance* and *cost*. These three are often mutually exclusive.

Network processor are usually located in a line card between a switching fabric and a media interface.

The network processors use parallelism, pipelines, optimised instruction set and specialiced coprocessors to achieve high speed.

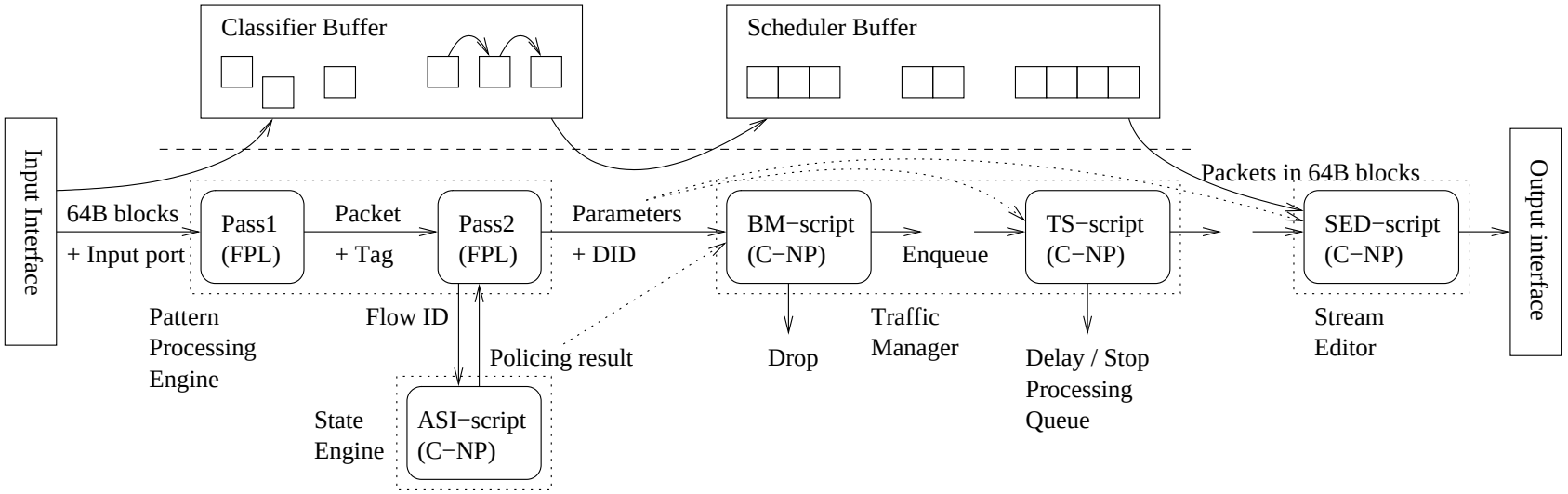



Example of an parallel architecture: Intel IXP2850 network processor.




Example of an pipelined architecture: Agere APP550 network processor.

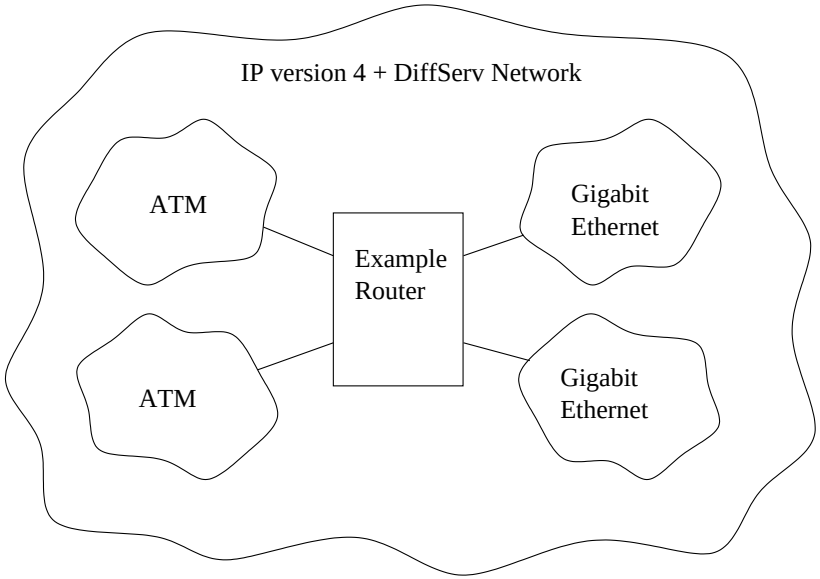
# APP550 program architecture




- Classifier: two passes, classification language FPL.
- VLIW engines: statistics, buffer management, traffic shaping, packet modification, C-NP simplified C language.
- Pipelined nature $\rightarrow$ execution time limited.

# Example router – Requirements

- Uses Agere APP550
- 2 ATM interfaces
- 2 Ethernet interfaces
- Diffserv routing. (*no* marking)



# Example router – Design

Not all functionality is possible to implement in the network processor. Slow path processing in the controlling host processor is needed.

1. Requirements are analysed to derive the external packet formats and functionality in the logical level.
2. Scheduling hierarchy is designed and the interface between the classifier and traffic manager is decided.
3. Policing, buffer management and traffic shaping uses algorithms from the reference: dual token bucket, weighted random early detection (WRED), modified weighted round robin (WRR).
4. Classifier is programmed in two passes.

# Example router – Testing

Testing is done with the simulator. The simulation runs can be automated, which helps in repeating tests and performing long test runs.

- Verifying specific functionality with individual packets.
- Testing QoS differentiation and performance with traffic flows.

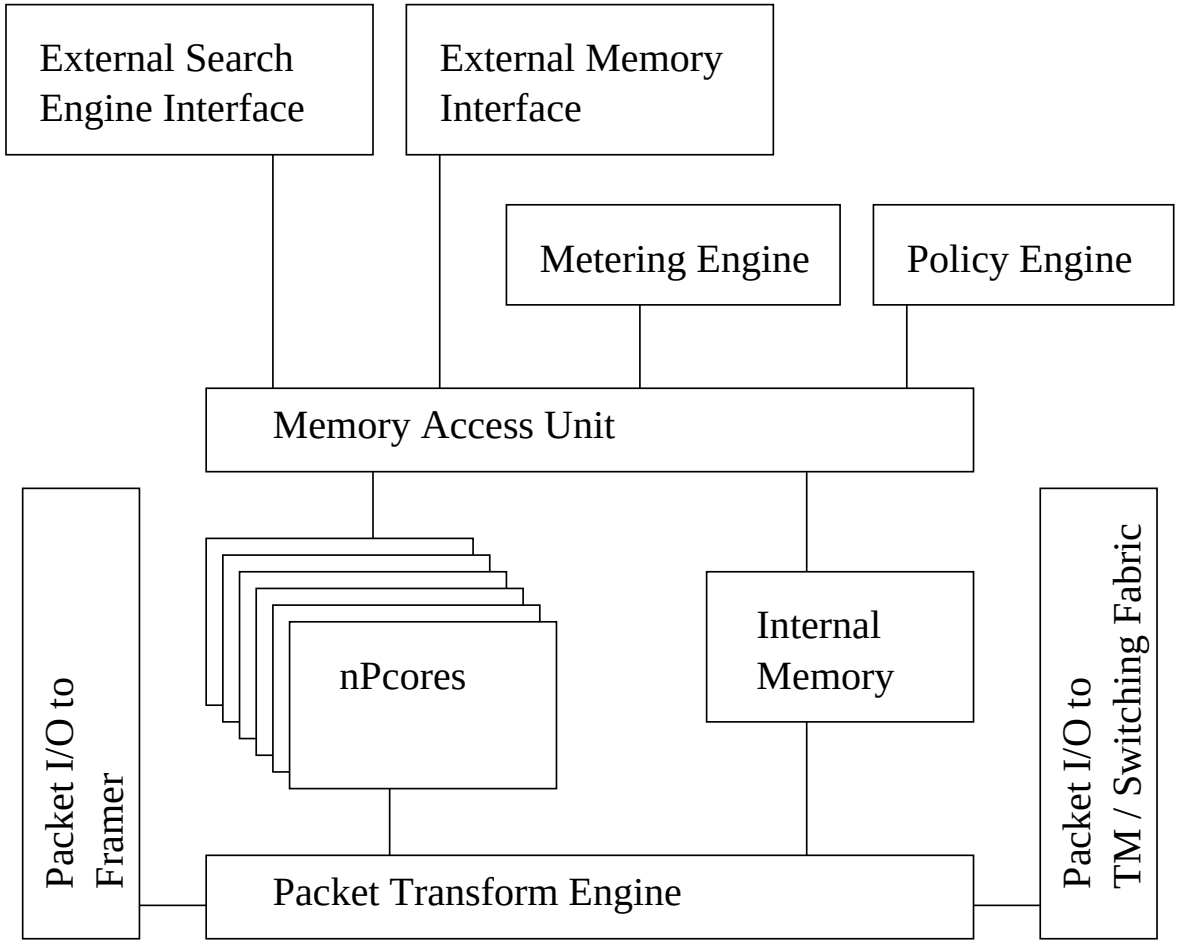
# Conclusion

The network processors look like a practical base for an IP router. However, new technology and an abundance of options require careful evaluation on a case-by-case basis.

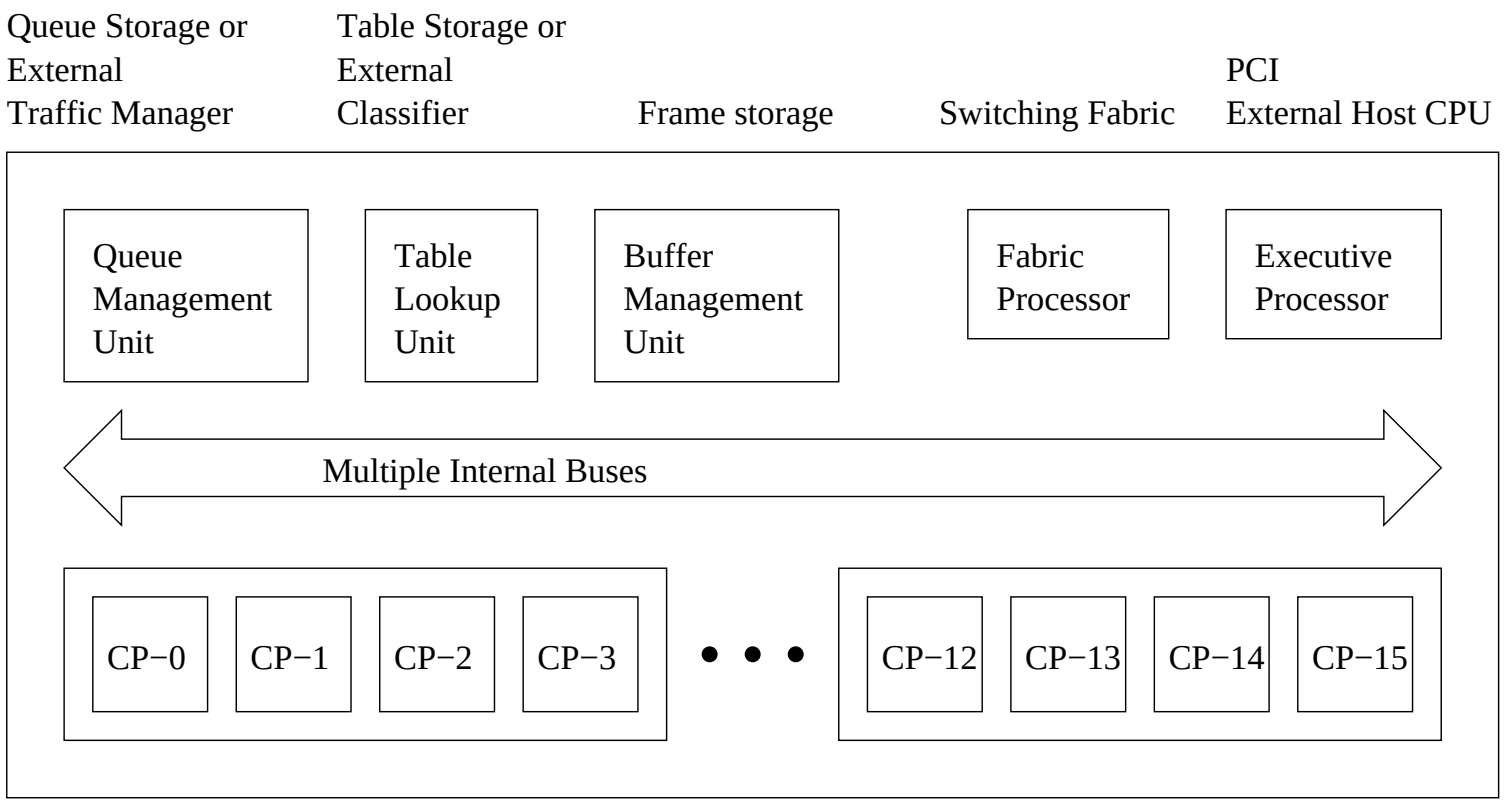
# Future work

- Requirements for other parts of 3GPP system (e.g. IMS).
- Host software in the example implementation.
- Processing for higher layers than IP. (This is challenging for the network processors, because in addition to a fast processing also a capability to keep packets a long time is needed.)

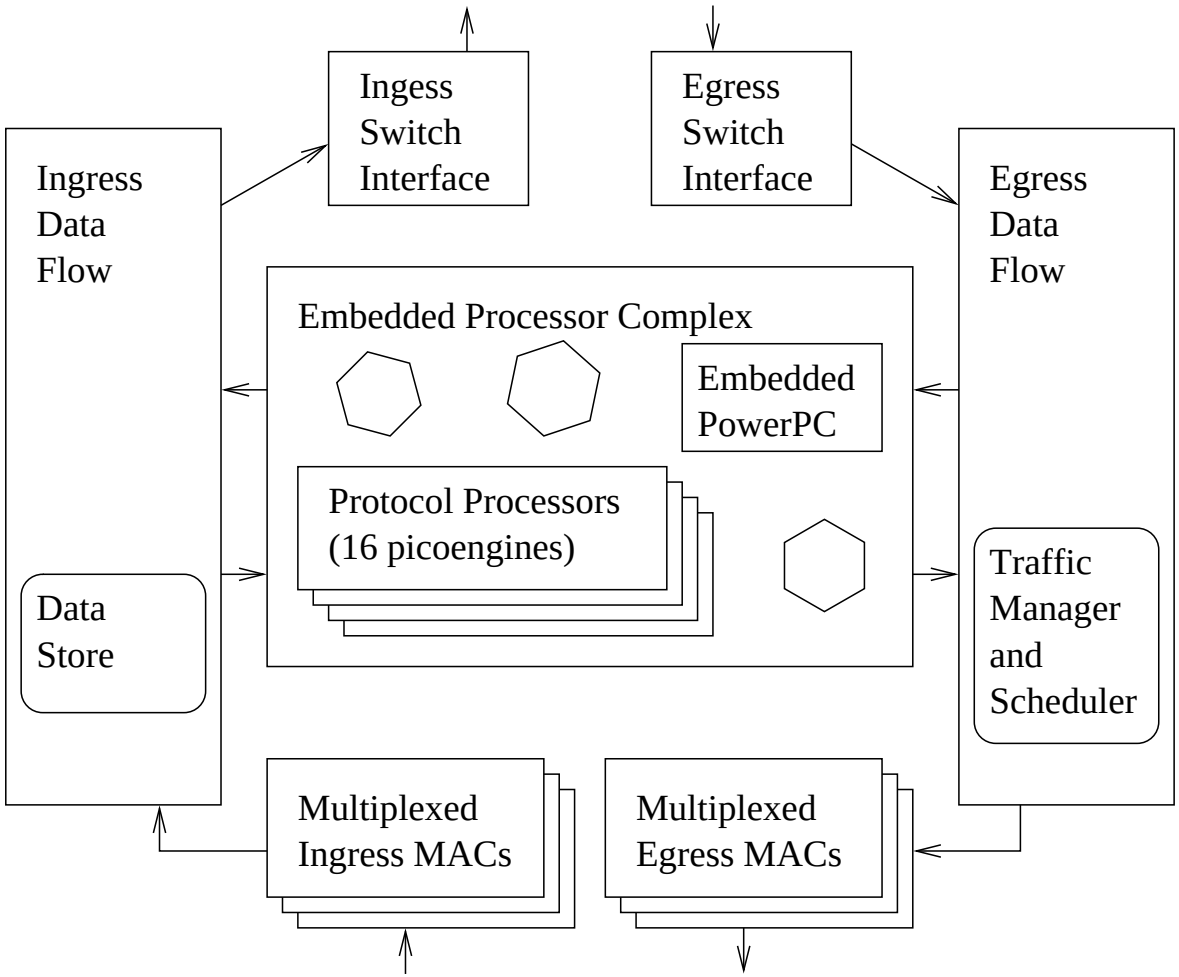
# Various NP architectures



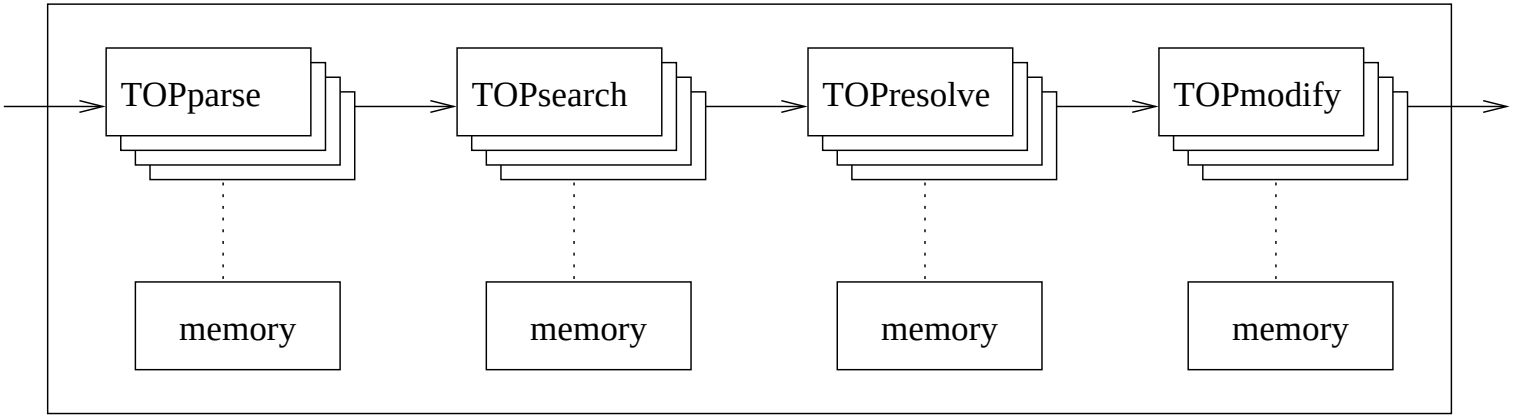

A simplified structure of a AMCC nP7510 network processor. (TM=Traffic Manager)



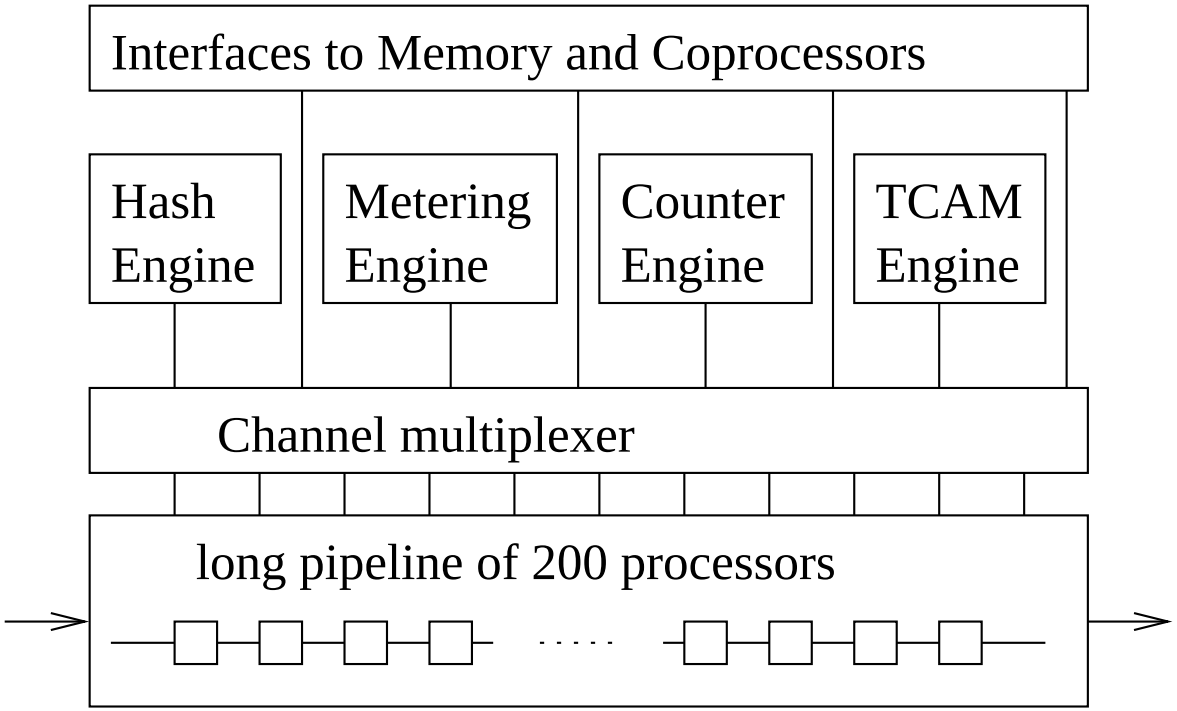

A block diagram of a C-Port C-5e architecture.



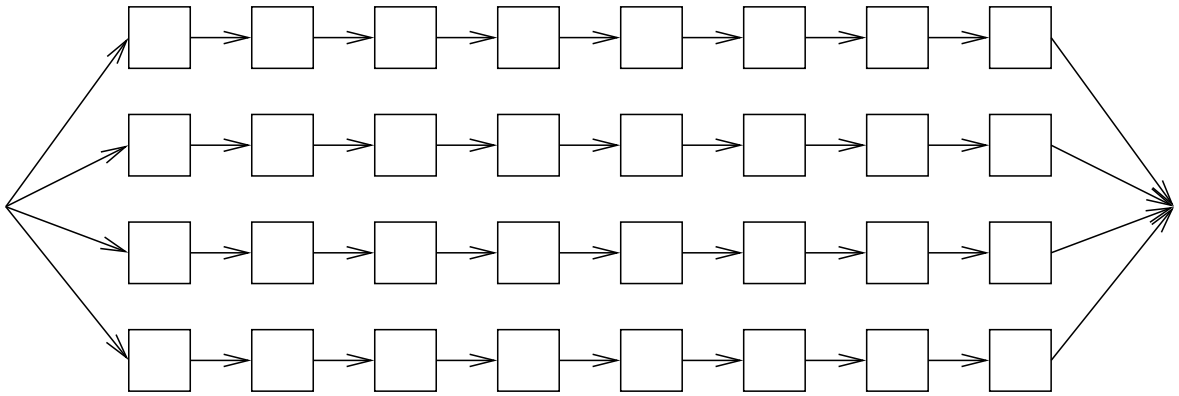

Architecture of a Hifn network processor chip.




Architecture of a EZchip NP-1c network processor.




Architecture of the Xelerated X10q network processor.



Cisco PXF network processor with 32 packet engines partitioned to four pipelines.